CLAIMS:

What is claimed is:

1. A polysilicon resistor comprising:

a first interlayer dielectric layer overlying a substrate;

a polysilicon region formed in said interlayer dielectric;

a first contact region extending down from a surface of said first interlayer dielectric;

a second contact region extending down from said surface of said first interlayer dielectric;

a first contact connected to said first contact region;

a second contact connected to said second contact region; and

a third contact connected to a surface of said polysilicon region, wherein said third contact is located between said first contact and said second contact, wherein said third contact forms a Schottky diode such that application of a voltage to said third contact forms a depletion region that changes in size depending on a voltage applied to said third contact, thereby changing a resistance in said depletion resistor.

2. The polysilicon resistor of claim 1, wherein said third contact is connected to said surface by a salicided region.

3. The polysilicon resistor of claim 1, wherein said polysilicon region is doped with an n-type doping.

4. The polysilicon resistor of claim 3, wherein said first contact region and said second contact region are n+ contact regions.

5. The polysilicon resistor of claim 1, wherein said first contact, said second contact, and said third contact are formed using metal layers.

6. The polysilicon resistor of claim 5, wherein the metals layers are tungsten metal layers.

7. The polysilicon resistor of claim 1, wherein said polysilicon region contains n-type dopants having a concentration of about 1 x $10^{15}/cm^3$.

8. The polysilicon resistor of claim 1, wherein said first contact region and said second contact region contain n-type dopants having a concentration of about 1 x $10^{18}/cm^3$ to about 1 x $10^{20}/cm^3$.

9. A chip comprising:

a substrate on which a plurality of elements of an integrated circuit are formed;

a first interlayer dielectric layer overlying said substrate;

a polysilicon region formed in said interlayer dielectric;

a first contact region extending down from a surface of said first interlayer dielectric;

a second contact region extending down from said surface of said first interlayer dielectric;

a first contact connected to said first contact region;

a second contact connected to said second contact region; and

a third contact connected to a surface of said polysilicon region, wherein said third contact is located between said first contact and said second contact, wherein said third contact forms a Schottky diode such that application of a voltage to said third contact forms a depletion region that changes in size depending on a voltage applied to said third contact, thereby changing a resistance in said depletion resistor;

wherein said polysilicon region forms a resistor for said integrated circuit.

10. The chip of claim 9, wherein said third contact is connected to said surface by a salicided region.

11. The chip of claim 9, wherein said polysilicon regions is doped with an n-type doping.

12. The chip of claim 11, wherein said first contact region and said second contact region are n+ contact regions.

13. The chip of claim 9, wherein said first contact, said second contact, and said third contact are formed using metal layers.

14. The chip of claim 13, wherein the metals layers are tungsten metal layers.

15. The chip of claim 9, wherein said polysilicon region contains n-type dopants having a concentration of about $1 \times 10^{15}/cm^3$.

16. The chip of claim 9, wherein said first contact region and said second contact region contain n-type dopants having a concentration of about $1 \times 10^{18}/cm^3$ to about $1 \times 10^{20}/cm^3$.

17. A method for forming a polysilicon resistor, the method comprising:

forming a doped polysilicon region in a interlayer dielectric layer;

forming a first contact region and a second contact region in said doped polysilicon region, wherein said first contact region and said second contact region extend downward from a surface of said polysilicon;

forming a first contact on said first contact region and a second contact on said second contact region; and

forming a third contact on a surface of said doped polysilicon region, wherein said third contact is located between said first contact and said second contact, wherein said third contact forms a Schottky diode such that application of a voltage to said third contact forms a depletion region that changes in size depending on a voltage applied to said third contact, thereby changing a resistance in said depletion resistor.

18. The method of claim 17, wherein said step of forming said doped polysilicon region comprises:

removing a given region of an interlayer dielectric layer;

filling said given region with polysilicon;

implanting n-type dopants into said polysilicon.

19. The method of claim 18, wherein said n-type dopants implanted into said polysilicon region have a concentration of about 1 x $10^{15}/cm^3$

20. The method of claim 18, wherein a doping profile of the n-type dopants is selected to reduce parasitic capacitance.

21. The method of claim 18, wherein the step of forming said first contact region and said second contact region comprises:

implanting n-type dopants into portions of said polysilicon region in a concentration of about 1 x $10^{18}/cm^3$ to about 1 x $10^{20}/cm^3$.

22. The method of claim 18, wherein the step of forming said first contact and said second contact comprises:

depositing a metal layer onto said first contact region and said second contact region.

23. The method of claim 22, wherein said metal layer is a tungsten metal layer.

24. The method of claim 18, wherein said doped polysilicon region receives an n-type doping.